ADC and DAC Glossary

This document summarizes commonly used terms when dealing with analog-to-digital converters (ADCs) and digital-to-analog converters (DACs).

A

acquisition time
Acquisition time is used when dealing with the track-and-hold input circuitry of an ADC. It is defined as the time between releasing the hold state of the track-and-hold input circuitry and the output of the sample circuit settling to the new input voltage value during the track mode. The acquisition time (T_{acq}) for the analog input to settle to within 1 LSB is given by the following equation:

$$T_{acq} = \ln(2^N) \times (R_{SOURCE} \times C_{SAMPLE})$$

where R_{SOURCE} is the source impedance, C_{SAMPLE} is the sampling capacitance, and N is the number of bits of resolution.

aliasing
In sampling theory, when an input signal frequency component exceeds the Nyquist limit, the signal is "aliased" or "folded back" or replicated at other frequencies in the frequency spectrum above and below Nyquist. Normally, aliasing is due to unwanted signals beyond the Nyquist limit. To prevent aliasing, all undesired signals must be filtered adequately so that they are not digitized by the ADC. Aliasing can be used advantageously when undersampling.

See also application note *Filter Basics: Anti-Aliasing*

aperture delay
Aperture delay (t_{AD}) in an ADC is the time defined between the sampling edge (rising edge in Figure 1) of the clock signal and the instant when the actual sample is taken. The time when the actual sample is taken is when the ADC's track-and-hold goes into the hold state.

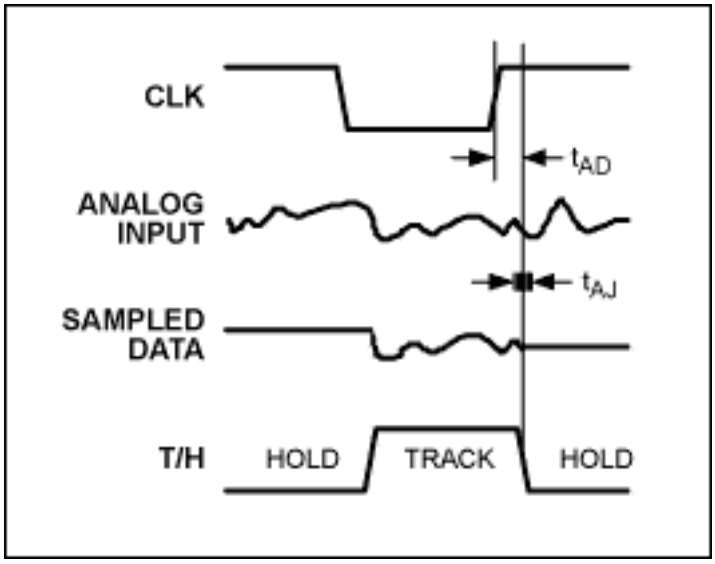

Figure 1. Aperture Delay and Jitter

aperture jitter
Aperture jitter (t_{AJ}) is the sample-to-sample variation in the aperture delay. See Figure 1. This value is typically much smaller than that of the aperture delay.

B

binary coding (unipolar)
In (straight) binary is a coding scheme typically used for unipolar signals. The binary code ranges from zero-scale to full-scale. Zero-scale is represented by all zeros (00...000) and positive full-scale is represented by all ones (11...111). Mid-scale is represented by a one (MSB) followed by all zeros (10...000). This is similar to offset binary, which is used for bipolar transfer functions (positive and negative values).

bipolar inputs
The term "bipolar" indicates that the signal swings above and below some reference point. In single-ended systems, the input is typically referenced to analog ground, so a bipolar signal refers to one that swings above and below ground. In differential systems, where the signal is not referenced to ground but where the positive input is referenced to the negative input, a bipolar signal is one in which the positive input swings both above and below the negative input, which is not necessarily analog ground.

C

common-mode rejection (CMR)
Common-mode rejection is the ability of a device to reject a signal that is "common" to both inputs. The common-mode signal can be either an AC or a DC signal or a combination of the two. Common-mode rejection ratio (CMRR) is the ratio of the differential signal gain to the common-mode signal gain. CMRR is often expressed in decibels (dB).

crosstalk
Crosstalk indicates how well each analog input is isolated from the others. For an ADC with more than one input channel, crosstalk is the amount of signal from one analog input that appears on the measured analog input. This value is typically specified in decibels. For a DAC with more than one input channel, crosstalk is the amount of noise that appears on a DAC output when another DAC output channel is updated.

D

differential nonlinearity (DNL) error
For an ADC, DNL error is defined as the difference between the ideal and the measured code transitions for successive codes. An ideal ADC would have finite digital codes exactly 1LSB apart (DNL = 0). For a DAC, DNL error is the difference between the ideal and the measured output value between successive DAC codes. An ideal DAC would have analog output values exactly one code apart (DNL = 0). A DNL specification of greater than or equal to 1LSB guarantees monotonicity (see monotonic).

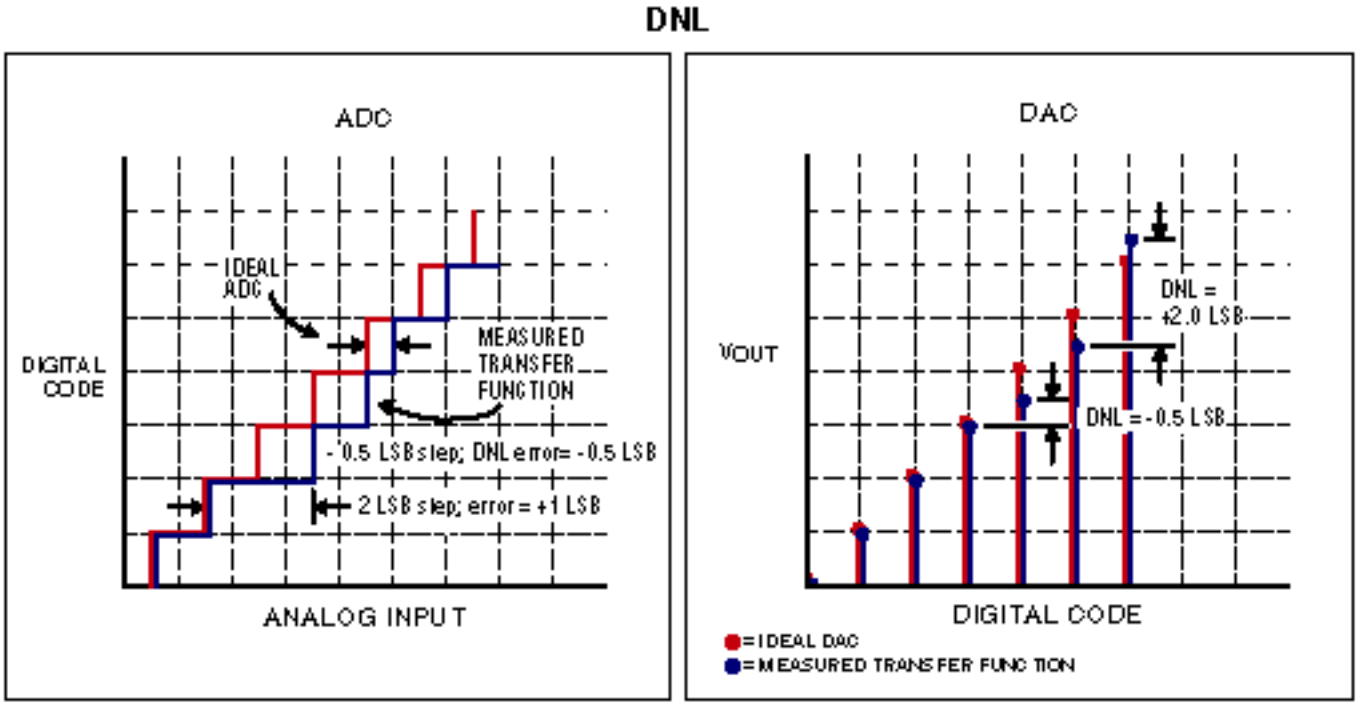

Figure 2. DNL for a) ADC and b) DAC

See also application note *INL/DNL Measurements for High-Speed Analog-to-Digital Converters (ADCs)*

digital feedthrough
Digital feedthrough is the amount of noise that appears on the DAC output when the digital control lines are toggled. In Figure 3, the feedthrough on the DAC output is the result of the noise from the serial clock signal.

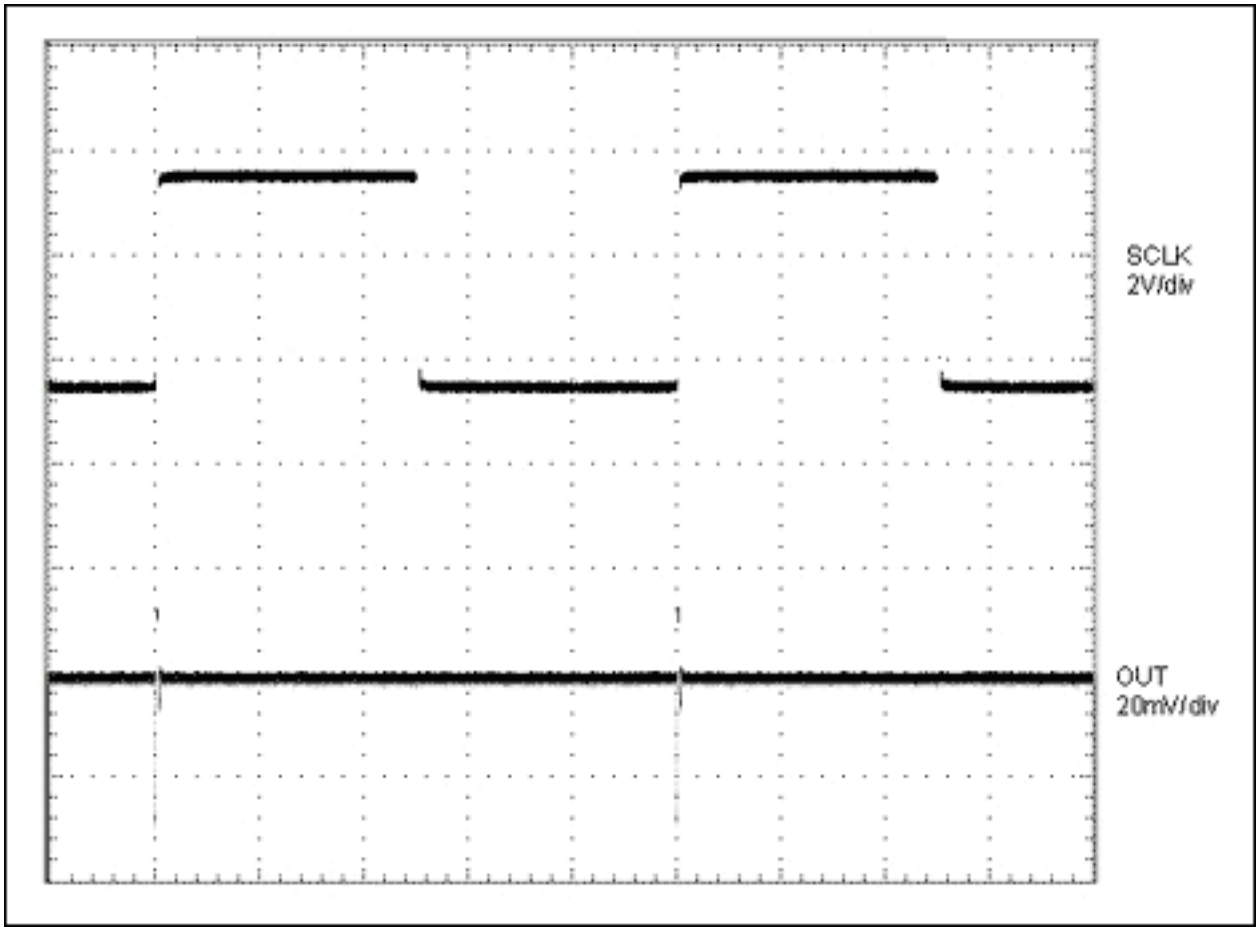

Figure 3. Digital Feedthrough

dynamic range
Typically expressed in dB, dynamic range is defined as the range between the noise floor of a device and its specified maximum output level. The dynamic range of an ADC is the range of signal amplitudes the ADC can resolve. An ADC with a dynamic range of 60dB means that it can resolve signals with amplitudes from x to 1000x. Dynamic range is important in communication applications where signal strengths vary dramatically. If the signal is too large, it will over-range the ADC input. If the signal is too small, the signal will get lost in the quantization noise of the converter.

E

effective number of bits (ENOB)
ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of only quantization noise. As the input frequency increases, the overall noise (particularly in the distortion components) also increases, thereby reducing the ENOB and SINAD (see signal-to-noise and distortion ratio). ENOB for a full-scale sinusoidal input waveform is computed from:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

F

force-sense outputs
DACs with integrated output amplifiers sometimes provide force-sense outputs. This means that the inverting input of the output amplifier is available for external connection and the feedback path must be closed externally.

full-power bandwidth (FPBW)
A large-signal (at or near full-scale) analog input is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB. This point is defined as the full-power input bandwidth frequency.

full-scale (FS) error
For an ideal ADC, the code edge triggers the transition to full-scale at 1.5LSB below the full-scale analog voltage. The full-scale error is the difference between this ideal code transition and the actual measured code transition. Full-scale error = offset error + gain error. See Figure 4.

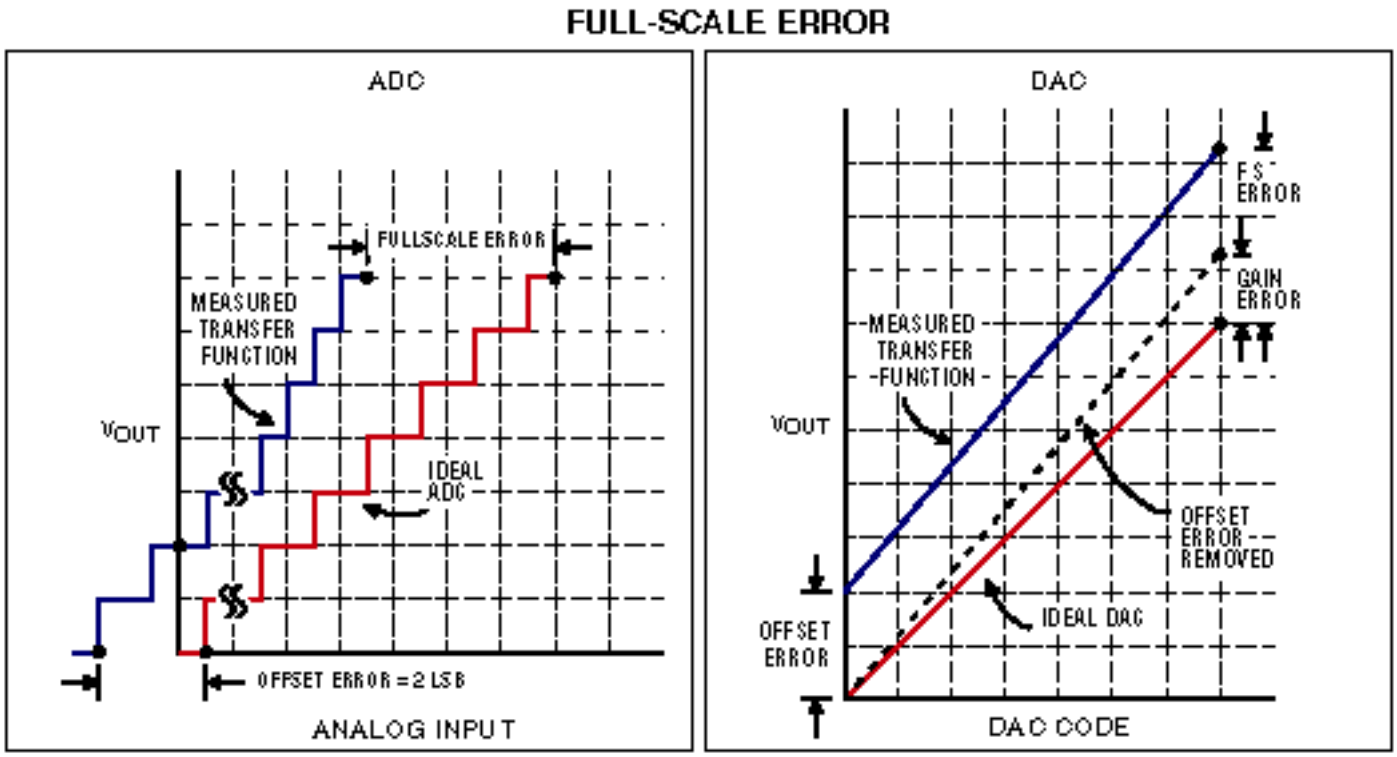

Figure 4. Full-Scale Error for a) ADC and b) DAC

G

gain error

Gain error is a figure of merit that indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed in LSB or a percent of full-scale range (%FSR). It can be calibrated out with hardware or in software.

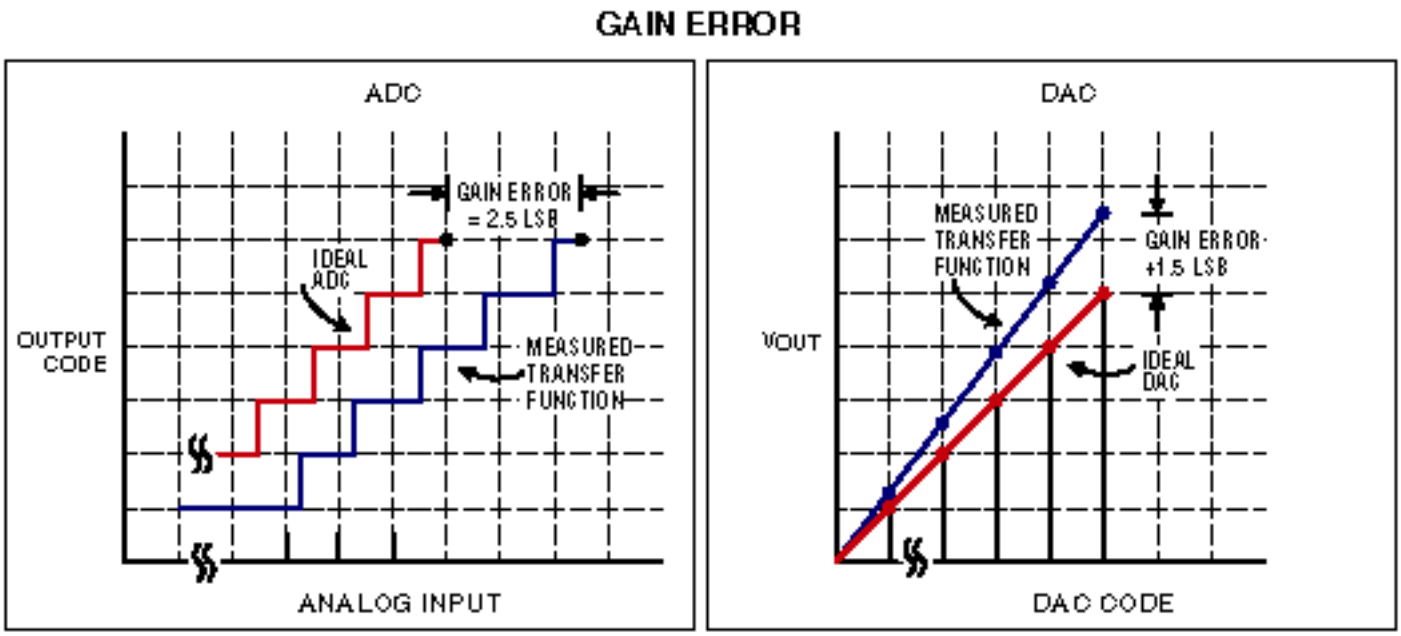

Figure 5. Gain Error for a) ADC and b)DAC

gain error drift
Gain error drift is the variation in gain error due a change in ambient temperature. This is typically expressed in ppm/° C.

gain matching
Gain matching is a figure of merit that indicates how well the gain of all channels in a multiple-channel ADC are matched to each other. The same input signal is applied to all channels and the maximum deviation in gain is reported (typically in dB) as gain matching.

glitch impulse energy (also major-carry transition glitch energy)
Glitch impulse energy is the amount of energy that appears at the DAC output when a major-carry transition occurs. It is measured typically in nV*s and given by the area under the curve on a voltage vs. time graph.

H

harmonic
A harmonic is a frequency component of a sine-wave that is a multiple of the fundamental frequency.

I

integral nonlinearity (INL) error
INL is the deviation of the values on an actual transfer function from a straight line. This straight line is either a best-fit straight line or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. "Relative accuracy" is a term often used to refer to INL. Maxim typically uses the end-point method when specifying INL for data converters. The end-point method is the more conservative of the two methods and is typically 2x better than the best-fit straight line method.

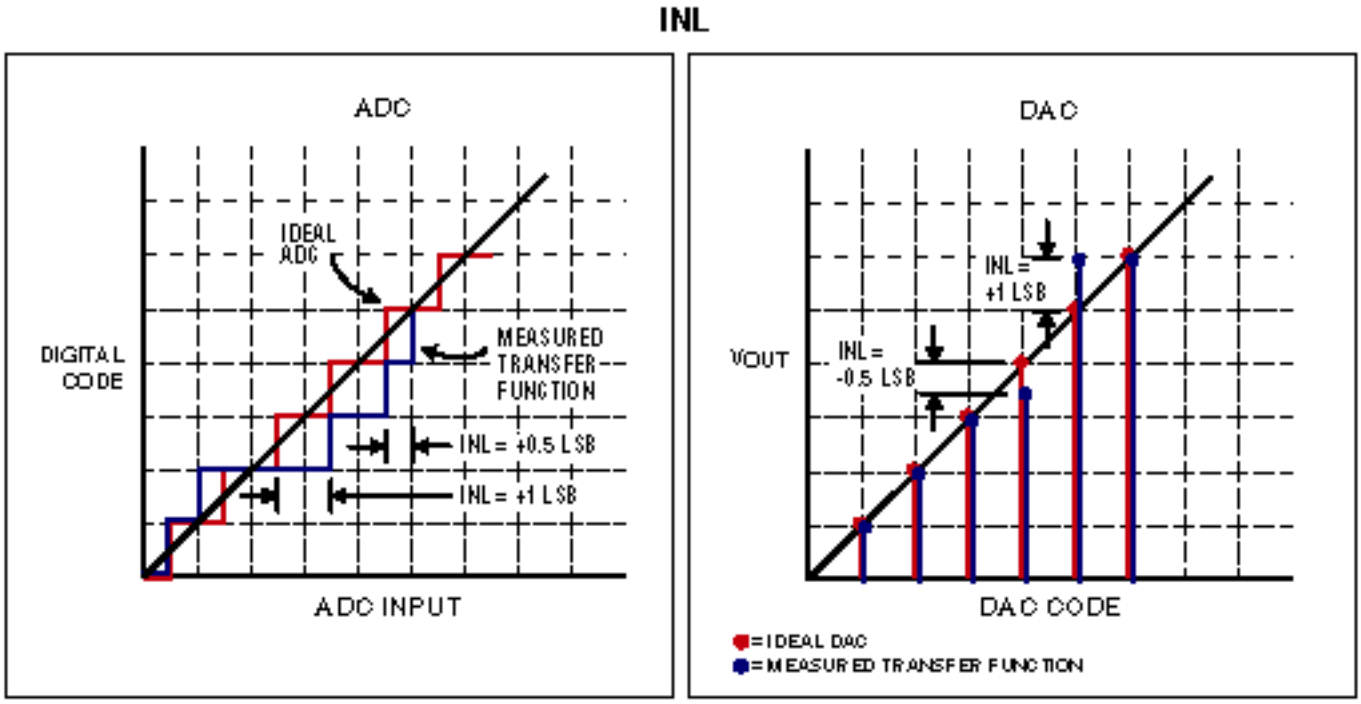

Figure 6. INL for a) ADC and b) DAC

See also application note *INL/DNL Measurements for High-Speed Analog-to-Digital Converters (ADCs)*

intermodulation distortion (IMD)
IMD is an RF signal defect in which non-linear circuits or devices create new frequency components not in the original signal, including the common harmonic and two-tone distortion effects. It is measured as the total power of the selected intermodulation products (ie. IM2 through IM5) to the Nyquist frequency relative to the total input power of the two input signal, f1 and f2. f1 and f2 are of equal amplitude and are very close to one another in frequency. The 2nd-5th order intermodulation products are as follows:

- 2nd order intermodulation products (IM2): f1 + f2, f2 - f1
- 3rd order inter modulation products (IM3): 2 x f1 - f2, 2 x f2 - f1, 2 x f1 + f2, 2 x f2 + f1
- 4th order inter modulation products (IM4): 3 x f1 - f2, 3 x f2 - f1, 3 x f1 + f2, 3 x f2 + f1
- 5th order inter modulation products (IM5): 3 x f1 - 2 x f2, 3 x f2 - 2 x f1, 3 x f1 + 2 x f2, 3 x f2 + 2 x f1

L

least significant bit (LSB)
In a binary number, the LSB is the least weighted bit in the group. Typically, the LSB is the furthest-right bit. For an ADC or DAC, the full-scale voltage range of the converter divided by 2N, where N is the converter's resolution, determines the weight of an LSB. For example, for a 12-bit, ADC with a unipolar full-scale voltage of 2.5V, 1 LSB = (2.5V/212) = 610µV.

M

major-carry transition
Major-carry transition is the point around mid-scale where the MSB changes from low to high and all other bits change from high to low, or where the MSB changes from high to low and all other bits change from low to high. For example, 01111111 to 10000000 is a major-carry transition. This point is often where the worst switching noise occurs.

monotonic
A sequence increases monotonically if for every n, Pn + 1 is greater than or equal to Pn. Similarly, a sequence decreases monotonically if for every n, Pn + 1 is less than or equal to Pn. A DAC is said to be monotonic if the analog output always increases as the DAC code input increases. An ADC is said to be monotonic if the digital output code always increases as the ADC analog input increases. A ±1LSB DNL guarantees that a converter is monotonic.

most significant bit (MSB)
In a binary number, the MSB is the most weighted bit in the group. Typically, the LSB is the furthest-left bit.

multiplying DAC (MDAC)
A multiplying DAC is one that allows an AC signal to be applied to the reference input. This allows the DAC to be used as a digital attenuator by feeding the signal of interest into the reference input and using the DAC codes to scale the signal.

N

no missing codes
An ADC has no missing codes if a ramp signal is applied to the analog input and all digital codes appear in output data.

Nyquist frequency
The Nyquist principle states that the sampling rate of an ADC must be at least twice the maximum bandwidth of the analog signal in order to allow the signal to be completely represented with no aliasing effects. This is called the Nyquist frequency.

O

offset binary coding
Offset binary is a coding scheme often used for bipolar signals. In offset binary coding, the most negative value (negative full-scale) is represented by all zeros (00...000) and the most postive value (positive full-scale) is represented by all ones (11...111). Zero-scale is represented by a one (MSB) followed by all zeros (10...000). This is similar to straight binary, which is typically used for unipolar signals.

offset error (bipolar)
Offset error in bipolar converters is measured similarly to the offset error in unipolar converters. However, the error measured at zero-scale is at the midpoint of the bipolar transfer functions. See offset error (unipolar).

offset error (unipolar)
Offset error, often called "zero-scale" error, is a figure of merit that indicates how well the actual transfer function matches the ideal transfer function at a single point. For an ideal data converter, the first transition occurs at 1/2 LSB above zero. For an ADC, the zero-scale voltage is applied to the analog input and is increased until the first transition occurs. For a DAC, loading a code of all zeros into the DAC and measuring the analog output voltage determine the offset error.

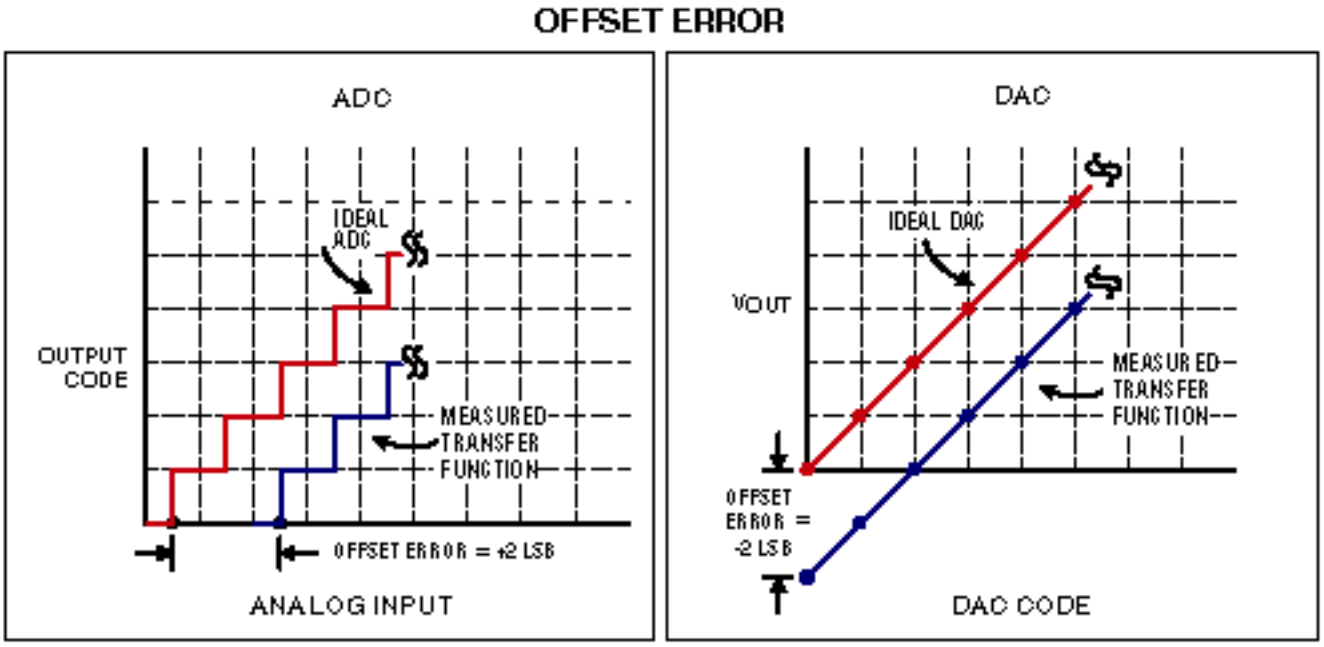

Figure 7. Offset Error for a) ADC and b) DAC

offset error drift
Offset error drift is the variation in offset error due a change in ambient temperature. This is typically expressed in ppm/° C.

oversampling
For an ADC, sampling the analog input at a much higher frequency than Nyquist is called oversampling. This technique improves the dynamic performance of the ADC by effectively reducing the noise floor of the converter. In turn, improved dynamic performance leads to higher resolution. Oversampling is the basis of sigma-delta ADCs.

See also application note *Demystifying Sigma-Delta ADCs*

P

phase-matching
Phase matching is a figure of merit that indicates how well the phase of all channels in a multiple-channel ADC is matched to each other. The same input signal is applied to all channels and the maximum deviation in phase is reported (typically in degrees) as phase matching.

power-supply rejection (PSR)
PSR is a measure of the data converter's level of immunity to power supply fluctuations. PSR assumes that the converter's linearity is unaffected by changes in the power-supply voltage. Power-supply rejection ratio (PSRR) is the ratio of the input signal change to the change in the converter output. PSRR is typically measured in dB.

Q

quantization error
Quantization is the process whereby the continuous range of input signal values is divided into nonoverlapping subranges. Each of these subranges has a discrete value of the output uniquely assigned. Once a signal value falls within a given subrange, the output provides the corresponding discrete value. For an ADC, quantization error is defined as the difference between the actual analog value and the digital representation of that value.

R

ratiometric measurement
Rather than using a voltage reference with an absolute value, a ratio of the signal applied to the transducer (ie. load cell or bridge) is also applied to the voltage reference input of the ADC, thereby eliminating any errors introduced by a changing reference. This type of measurement is referred to as ratiometric. Figure 8 provides an example of ratiometric measurement using a resistive bridge.

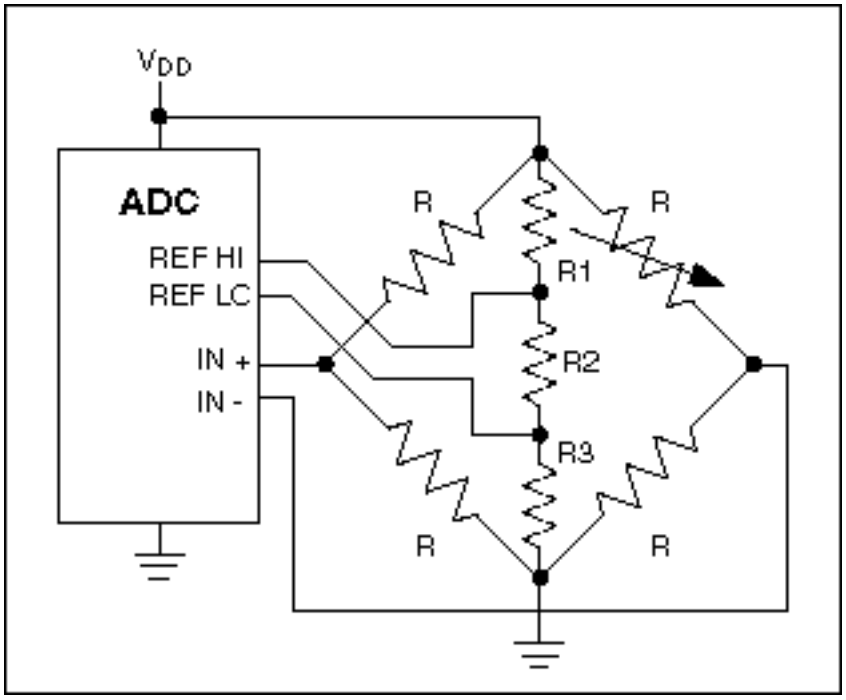

Figure 8. Ratiometric Measurement Using Resistive Bridge Network resolution

For an ADC, resolution is the number of bits that are used to represent the analog input signal. To more accurately replicate the analog signal, the resolution must be increased. Using ADCs with higher resolutions will reduce the quantization error. For DACs, the definition for resolution is similar but reversed. Incrementing the code in a DAC with higher resolution will result in smaller step sizes in the analog output.

root mean square (RMS)
RMS represents the effective DC value that an AC signal represents. For a sine wave, the RMS value is √2/2 (or 0.707) times the peak value, or 0.354 times the peak-to-peak value.

S

sampling rate/frequency
Sampling rate or frequency is the rate at which the ADC acquires, or samples, the analog input. It is specified as samples per second (sps) or Hertz (Hz). For ADCs that perform one sample per conversion (such as SAR, flash, and pipeline ADCs), the sampling rate is also referred to as the throughput rate. For sigma delta ADCs, the sampling rate is typically much higher than the output data rate.

settling time
Settling time is the amount of time it takes a DAC output to reach its final value (within a specified percentage) once the DAC has been commanded to change its output value. This time can be affected by the slew rate of an output amplifier and by the amount of amplifier ringing and signal overshoot. For an ADC, it is important that the time is takes for the voltage on the sampling capacitor to settle to within 1 LSB of the converter's acquisition time. See acquisition

time definition.

signal-to-noise and distortion (SINAD)
SINAD is the RMS value of the sine wave (input for an ADC and reconstructed output for a DAC) to the RMS value of the converter noise plus distortion. RMS noise plus distortion includes all spectral components up to Nyquist, excluding the fundamental and the DC offset. SINAD is typically expressed in dB.

signal-to noise ratio (SNR)
SNR is the ratio of the amplitude of the desired signal to the amplitude of the noise signals at a given point in time. For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum ADC noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[MAX]} = 6.02_{dB} \cdot N + 1.76_{dB}$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc.

signed binary coding
Signed binary is a coding scheme in which the MSB represents the sign (positive or negative) of a binary number. In this scheme, the 8-bit representation of "-2" is 10000010 and the representation of "+2" is 00000010.

slew rate
Slew rate is the maximum rate at which the DAC output can change, or the maximum rate at which an input signal can change without resulting in an error in the digitized representation of the input signal. For DAC with output amplifiers, the specified slew rate is typically the slew rate of the amplifier.

small-signal bandwidth (SSBW)
A small analog input signal is applied to an ADC in such as way that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB. The SSBW is often limited by the track-and-hold amplifier performance.

spurious-free dynamic range (SFDR)
SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset. SFDR is specified in decibels relative to the carrier (dBc).

T

total harmonic distortion (THD)
THD is a measure of the signal's distortion content. For ADCs, THD is the ratio of the RMS sum of the selected harmonics of the input signal to the fundamental itself. Only harmonics within the Nyquist limit are included in the measurement. THD is specified in decibels relative to the carrier (dBc). The following expression uses the first six harmonics to calculate the THD:

$$THD = 20 \cdot \log \left[\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2}}{V_1} \right]$$

track-and-hold
Track-and-hold, often called "sample-and-hold," refers to the input sampling circuitry of an ADC. The most basic representation of a track-and-hold input is an analog switch and a capacitor. See Figure 9. The circuit is in "track" mode when the switch is closed. When the switch opens, the last instantaneous value of the input is held on the sampling capacitor, and the circuit is in "hold" mode.

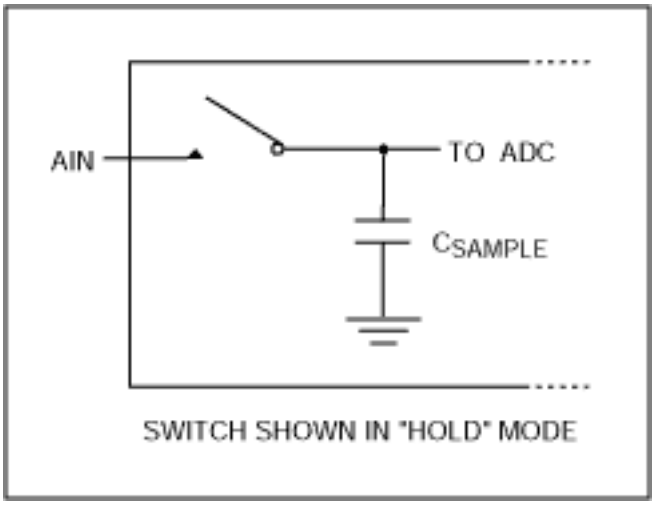

Figure 9. Basic Track-and-Hold

transition noise
Transition noise is the range of input voltages that cause the ADC result to toggle between output codes. As the analog input voltage is increased, the voltage that defines where a code transition occurs (code edge) has an associated amount of noise due to this transition.

two's complement coding
Two's complement is a digital coding scheme for negative numbers that simplifies addition and subtraction computations. In this scheme, the 8-bit representation of -2 is 11111110 and the representation of +2 is 00000010.

U

undersampling
Undersampling is a technique in which the ADC sampling rate is lower than the analog input frequency, which causes aliasing. Given the Nyquist criterion, it is natural to expect that undersampling would result in a loss of signal information. However, with proper filtering of the input signal and proper frequency selection of the analog input and sampling frequencies, the aliased components that contain the signal information can be shifted from a higher frequency to a lower frequency and then converted. This method effectively uses the ADC as a downconverter by shifting higher bandwidth signals into the ADC's desired band of interest. The bandwidth of the ADC's track-and-hold must be capable of handling the highest frequency signals for this technique to be successful.

unipolar
A unipolar signal is one that swings from zero to positive full-scale, thus having only a positive polarity. For a single-ended analog input of an ADC, the input ranges from zero-scale (typically ground) to full-scale (typically the reference voltage). For a unipolar ADC with differential inputs, the positive input swings from zero-scale (the negative input) to positive full-scale (with respect to the negative input).

Z

zero-scale error
See offset error (unipolar).